

Contents

1	Introduction	1
2	Field Programmable Gate Array basics	5
2.1	Generic structure	5
2.2	Typical applications	10
2.3	Existing designs	12
2.3.1	Related academic research	12
2.3.2	Commercial FPGAs	15
2.4	New approach in this thesis	21
3	Aspects of low power applications	23
3.1	Motivation	23
3.2	Static power dissipation	28
3.3	Dynamic power dissipation	30
3.4	Leakage current suppression	31
4	Cryptography and its application	35
4.1	Basic principles	35
4.2	Side channel attacks	35
4.3	Power Analysis	36
4.3.1	Simple Power Analysis	36
4.3.2	Differential Power Analysis	37
4.4	Countermeasures	38
5	Low-power configuration random access memory	41
5.1	Existing designs	41
5.2	New low-power approach: LP 4T SRAM Cell	61
5.2.1	Dual threshold CMOS	62
5.2.2	Transistor stacking	63
5.2.3	Dynamic voltage scaling	67
5.3	Timing considerations	72
5.4	Conclusion	74
6	Low-power data flip-flop	77
6.1	Basic considerations	77
6.2	Selected legacy designs	79
6.3	New power saving modifications	89
6.3.1	Dual threshold CMOS	93
6.3.2	Multi-oxide technology	93

6.3.3	Clk- and power-gating	93
6.3.4	Stacking	94
6.4	Simulation results	94
6.5	Conclusion	102
7	Low power tristate buffer	105
7.1	Basic considerations	105
7.2	Legacy design	108
7.3	New low-power approaches	114
7.3.1	Power gating	114
7.3.2	Leakage current reduction	114
7.3.3	Subthreshold current reduction	116
7.3.4	Multi supply voltage	117
7.4	Low-power tristate buffer	117
7.5	Simulation results	137
7.6	Conclusion	138
8	Partial component integration	141
8.1	LUT design	142
8.2	SLICE design	157
8.3	GPIO design	161
8.4	Conclusion	164
9	Summary / Outlook	167
9.1	Summary	167
9.2	Outlook	168
A	CRAM - Additional Figures and Simulation Results	171
B	D-FF - Additional Figures and Simulation Results	175
C	Tristate Buffers - Additional Simulation Results	181
D	Partial SLICE Integration - Additional Figures and Simulation Results	189
List of figures		191
Bibliography		197