

Contents

Abstract	ii
Acknowledgements	iv
Glossary	viii
1 Introduction	1
1.1 State of the art and applications	3
1.2 Purpose of the work	9
1.3 Thesis outline	11
2 Memristor	14
2.1 How memristor works	15
2.2 Memristor model basic	16
2.3 Double barrier memristor devices	17
2.4 Conclusion	20
3 Memristor emulator and neuron	21
3.1 Resistive memristor emulator ASIC	22
3.1.1 Resistive memristor emulator: architecture and design	23
3.1.2 Circuit design	26
3.1.3 Multiplexed four emulator	33
3.1.4 Memristor model implemented on resistive emulator	36
3.1.5 Data processing on FPGA	38
3.1.6 Emulator measurement results	41
3.1.7 Multiplexed four emulator measurement	43
3.2 Switched capacitor based four memristors of resistor range 1 M Ω to 7 G Ω	44
3.2.1 Switched capacitor resistance	45
3.2.2 Non-overlapping clock	47
3.2.3 Switched capacitor simulation and realization of resistance	52
3.2.4 Practical issues with switched capacitor	53
3.3 Resistive switching versus capacitive switching comparison	54
3.4 Integrate and fire neuron	55
3.5 Integrate and fire neuron measurement	56

3.6	ASIC Floorplanning	58
3.7	Conclusion	59
4	Neuromorphic pattern recognition	60
4.1	Long-Term Potentiation (LTP) and Long-Term Depression (LTD)	61
4.1.1	Long-term potentiation	61
4.1.2	Long term depression	62
4.2	Synaptic plasticity	62
4.3	Memristive pattern recognition	62
4.4	Competition, homeostasis and variability	64
4.5	Simulation results	65
4.6	Memristor based neuromorphic versus digital computer approach	67
4.7	Conclusion	71
5	Neuron ASIC	72
5.1	Neuron floorplan	72
5.2	Integrate-and-fire neuron operation	73
5.3	Neuron circuit blocks	75
5.3.1	Operational amplifier	75
5.3.2	Comparator design	89
5.3.3	Spike generator and digital control	92
5.4	Neuron simulation	92
5.5	Neuron measurement	94
5.6	Conclusion	96
6	Neuron signaling and memristor integration with neuron ASIC	97
6.1	Neuron signaling	97
6.2	Memristor and neuron ASIC integration	99
6.2.1	Double barrier memristor	99
6.2.2	Memristor and neuron integration circuit	102
6.2.3	Memristive system measurement	104
6.3	Memristor retention issue	105
6.4	Conclusion	107
7	Conclusion and outlook	108
A	Description of emulator ASIC pins used for testing purpose	111
B	Description of neuron ASIC pins used for testing purpose	114
	Bibliography	116
	List of Figures	128

List of Tables

132